

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

STANISLAV P. BAJUK ET AL.

Serial No. : 10/604,071

Patent No.: 7,080,344

Issued: **JULY 18, 2006**

For: **CODING OF FPGA AND
STANDARD CELL LOGIC IN A
TILING STRUCTURE**

ATTY. DOCKET NO.: BUR920030051US1

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Examiner: **TUYEN P. TO**

Art Unit: 2825

Confirmation No.: 1070

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Applicant respectfully submits the enclosed proposed Certificate of Correction, which corrects clerical errors made by the U.S. Patent and Trademark Office in the Letters Patent No. **US 7,080,344 B2**, issued July 18, 2006.

Respectfully submitted,

956

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**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**Page 1 of 1

PATENT NO. : 7,080,344

APPLICATION NO.: 10/604,071

ISSUE DATE : July 18, 2006

INVENTOR(S) : Bajuk et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Claim 15, at column 7, line 10, delete "flexibleogic" and insert --flexible logic--.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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